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09/560,364	04/28/2000	Karen Lo	10002496-1	3565

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EXAMINER	
PERILLA, JASON M	
ART UNIT	**PAPER NUMBER**
2634	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/560,364	Applicant(s) LO ET AL.	
	Examiner Jason M Perilla	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *5 and 7-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *5 and 7-10* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-15 are pending in the application.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-4, 6, & 11-15, drawn to halting data strobes on a source synchronous link, classified in class 327, subclass 100.

II. Claims 5, & 7-10, drawn to debug data capture systems, classified in class 375, subclass 221.

3. The inventions are distinct, each from the other because:

The two inventions have separate status in the art demonstrated by their different classification because the halting of data strobes is performed by the means of a specific logic configuration and the debug system consists of a method of testing the transmission of signals. Each of the two inventions is patentable in view of the other. Further, the search required for one group is not required for the other.

4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Michael G. Verga on September 3, 2003 a provisional election was made without traverse to prosecute the invention of halting data strobes on a source synchronous link", claims 1-4, 6, & 11-15. Affirmation of this election must be made by applicant in replying to this Office

action. Claims 5, & 7-10 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Specification

6. The disclosure is objected to because of the following informalities:

Page 13, line 20 contains the first reference to 222-228 although only the even numbers inclusive to the range are identified in the drawings. The further references to 222-228 as well as the reference to 22-228 on page 23, line 11 are also objected to.

Page 14, line 2 contains the reference STOP_STB_HIGH 220, although the drawing contains STOP_DS_HIGH 220.

Page 16, line 22 contains the reference 116 although 106 is used in the drawings.

Page 23, lines 14 & 16 both contain the reference 613 although 614 is used in the drawings.

Page 25, line 7 contains the reference GND_DS 228 although 226 is used in the drawings.

Page 33, line 5 contains the reference 100 although 1006 is appropriate.

Page 33, line 12 contains the reference 1002 although 1002A is appropriate.

Page 33, line 29 contains the reference 110 although 1010 is appropriate.

Appropriate correction is required for each instance.

Claim Objections

7. Claims 2, 6, & 14 are objected to because of the following informalities:

Claim 2, line 3 recites "said first frequency" which lacks proper antecedent basis.

Claim 6, line 6 recites "said logic level signals" which lacks proper antecedent basis.

Claim 14, line 3 the phrase "said second of forth" should read "said second and forth".

Appropriate correction is required for each instance.

8. Claim 3 is dependent on claim 1 in the application. It appears that it should be dependent on claim 2 to provide proper antecedent basis for "said first data strobe signal" and "said second data strobe signal". Appropriate correction is required.

9. Claim 14 is dependent on claim 12 in the application. It appears that it should be dependent on claim 13 to provide proper antecedent basis for "said first and third input signals" and "said second and forth input signals". Appropriate correction is required.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-2, are rejected under 35 U.S.C. 102(b) as being anticipated by National Semiconductor DS26C31T/DS26C31M CMOS Quad TRI-STATE Differential Line Driver hereafter referred to as National.

Regarding claim 1, National discloses a source synchronous link comprising a communication link and a source synchronous receiver and transmitter coupled to the communication link. National further discloses data transmit logic to manage the transmission of data signals as well as data strobe logic configured to generate one or more data strobes that may be halted in a logical state in response to an external condition. The DS26C31 part is a transmitter. The drawing entitled "Logic Diagram" on page 4 shows both data and data strobe(s) transmit logic to be available on the DS26C31 chip by the four drivers as well as an input used to halt output of the data strobe(s) in a logical state by the means of the enable pins. The drawing entitled "Two-Wire Balanced System, RS-422" on page 6 shows a source synchronous receiver (DS26C32A) and transmitter (DS26C31) as well as a communication link (connecting wire). The drawing in view of the logic diagram implies multiple data/data strobe connections identical to the drawing making up the full communication link since the DS26C31 chip has multiple transmit logic components.

Regarding claim 2, National discloses data strobe signal(s) that comprise a first data strobe signal and a second data strobe signal that are transmitted with a phase opposite of each other (see description of differential line driver). Figure 2 shows the waveforms of the data strobe (OUTPUT) and the phase opposite waveform (/OUTPUT) to be transmitted.

12. Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Texas Instruments CDC111 1-Line to 9-Line differential LVPECL Clock Driver hereafter referred to as Texas Instruments.

Regarding claim 4, Texas Instruments discloses a synchronous transmitter for the transmission of a differential data strobe over a source synchronous link that toggles between one of two logical states in the normal mode of operation and with the differential data strobe signals held at one of the logical states when operating in a data capture debug mode of operation. The CDC111 part is a source synchronous transmitter. The logic diagram on page 2 shows the source synchronous transmitter with differential outputs and the function table on page 1 shows the normal mode of operation (/OE at low logic level) where the differential outputs toggle between one of two logical states and the debug mode of operation (/OE at high logic level) where the differential outputs are held at one of the two logical states.

13. Claims 6, & 11-15 are rejected under 35 U.S.C. 102(a) as being anticipated by Keeth et al (6026051).

Regarding claim 6, Keeth et al discloses a synchronous transmitter for the transmission of a differential data strobe over a source synchronous link that toggles between one of two logical states in the normal mode of operation and with the differential data strobe signals held at one of the logical states when operating in a data capture debug mode of operation as dependent on claim 4 (fig. 3; col. 3, line 45). Figure 3 shows the differential outputs DCLKOUT and /DCLKOUT making the circuit applicable as a transmitter. The /enable input to

the circuit is used to put the outputs at one logical state for data capture debug mode (col. 3, line 45). Keeth et al further discloses differential data strobe transmit logic (fig. 3, ref. 42 & 50), a differential data strobe signal generator configured to determine the logical states of the data strobe and inverse data strobe outputs (fig. 3, ref. 38, 40, 46, & 48; col. 3, line 45 – col 4, line 65), and strobe stopping logic utilized by the signal generator to halt the data strobe signals (fig. 3, ref. 36 & 44).

Regarding claim 11, Keeth et al discloses a data strobe transmitter for transmitting a differential strobe over a communications link that comprises a differential data strobe signal generator that determines a shape of the data strobe signal (fig. 3, ref. 38, 40, 46, & 48). Keeth et al further discloses strobe stopping logic configured to control signal level states used by the signal generator logic to cause the differential data strobe to remain in a desired logic state (fig. 3, ref. 38, 40, 46, & 48; col. 3, line 45 – col. 4, line 65).

Regarding claim 12, Keeth et al discloses the limitations as applied to claim 11 above, and further discloses the differential strobe signal generator logic selecting alternately between two applied signal levels to generate each of two differential data strobe signals. Figure 3 shows the differential strobe signal generator logic (ref. 38, 40, 46, & 48) having four applied signals used to generate the two differential data strobe signals. Keeth et al discloses that the two differential strobe outputs are each generated by selecting alternately between two of the applied signal levels (col. 3, line 45 – col. 4, line 65).

Regarding claim 13, Keeth et al discloses the limitations as applied to claim 12 above, and further discloses (col. 3, line 45 – col. 4, line 65) and shows in figure 3 that two applied signals levels (VCC & output of inverter 44) are used to generate strobe output DCLKOUT and two other applied signal levels (GND & output of inverter 36) are used to generate strobe output /DCLKOUT.

Regarding claim 14, Keeth et al discloses the limitations as applied to claim 12 above, and further discloses a first and third input signal to the differential data strobe generator held constantly in an asserted state (fig. 3, ref. VCC & the output of inverter 36) during normal operation as well as a second and forth input signal to the differential data strobe generator held constantly in a de-asserted state (fig. 3, ref. GND & the output of the inverter 44) during normal operation. Keeth et al also discloses that the differential signal generator selects alternately between the first and second input signals to generate the first data strobe signal and between the third and forth signals to generate the inverse data strobe signal (fig. 3; col. 3, line 45 – col. 4, line 65).

Regarding claim 15, Keeth et al discloses the limitations as applied to claim 12 above, and further discloses that the data strobe signal and the inverse data strobe signal are each generated as single ended bits that are opposite in phase with each other (col. 3, line 45 – col. 4, line 65).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to

be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over National in view of Texas Instruments.

Regarding claim 3, National disclosed a communication link and a source synchronous receiver and transmitter coupled to the communications link with data transmit logic as well as data strobe transmit logic that can be halted in response to an external condition as applied to claim 1. National further discloses a first and a second output of opposite phase with respect to each other that may take one of two logical states for the transmission of the data strobe during normal operation (fig. 2). National does not disclose the data strobe transmitter holding the data strobe signal at one of the logical states when operating in a debug mode of operation. However, Texas Instruments does disclose a differential data strobe transmitter that transmits in one of two logical states in normal operation and at one of the logical states when operating in a data debug mode. The function table on page 1 shows that the data strobe transmission logic transmits in one of the two logical states in normal operation (/OE at low logic level) and holds the data strobe transmission at one of the two logical levels when in the debug mode of operation (/OE at high logic level). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to modify the data strobe transmission logic of National to transmit one of two logical states used during normal operation when in debug mode because the data strobe transmission should

never be held in a state other than one of the two logical states used during normal transmission to ensure the proper interpretation of the data strobe signal at all times on the side of the receiver.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents and publications are cited to further show the state of the art with respect to halting data strobes.

U.S. Pat. No. 5852378 to Keeth et al; differential clock generator

National Semiconductor DS26C32A datasheet; quad differential line receiver

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (703) 305-0374. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (703) 305-4714. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-0377.

Jason M Perilla
September 4, 2003

STEPHEN CHIN
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